Title: Techniques for 2-D and 3-D Network-on-Chip (NoC) Design, Synthesis and Reconfiguration

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Summary: System-on-Chip (SoC) is a paradigm for designing today's integrated circuit (IC) chips that puts an entire system onto a single silicon floor (instead of printed circuit boards containing a number of chips accomplishing the system task). With the increasing number of cores integrated on such a chip, on-chip communication efficiency has become one of the key factors in determining the overall system performance and cost. The communication medium used in most of the modern Systems-on-Chip (SoCs) is shared global bus. In bus based Systems-on-Chip (SoC), due to many on-chip communication challenges, the performance, speed, and power consumption of a system can be affected severely. Network-on-Chip (NoC) is an emerging alternative that overcomes this bottleneck for integrating large number of cores on a single SoC. NoC is a specific flavor of interconnection networks where the cores communicate with each other using a router based packet switched network. Interconnection networks have been studied for more than last two decades and a solid foundation of design techniques has been reported in the literature. Thus, NoC is today becoming an emerging research and development topic including hardware communication infrastructure design, software and operating system services, CAD tools for NoC synthesis, reconfigurable design and so on. In designing NoC systems, there are several issues to be concerned with, such as topologies, routing algorithms, performance, latency, power consumption, complexity and so on. None of these factors can be independent in deciding the NoC architecture.

This tutorial aims at covering the important aspects of NoC design – communication infrastructure design, communication methodology, evaluation framework, mapping of applications onto NoC, topology synthesis etc. Apart from these, it also proposes to focus on other upcoming NoC issues, such as, reconfiguration, 3-D NoC design, and thermal aware NoC design.

Targeted Audience and Prerequisites: Final year graduate, postgraduate, and research students of Electronics/Electrical discipline intending to work on VLSI design. The tutorial will also cater to the design engineers working in chip design and CAD tool development. It requires a basic understanding of VLSI design process.

Keywords: VLSI Design Methodologies – Networks-on-Chip

Duration: 3 Hours (Half-day)

Detailed Tutorial Program: It is intended to cover the following topics with the estimated time distribution as noted next.

1. **Introduction (10 minutes):** Will present the evolution of NoC from SoC - its research and developmental challenges.
2. **NoC Protocols (20 minutes):** Will discuss on NoC protocols, elaborating flow control, available network topologies, routing mechanisms, fault tolerance, support for quality-of-service, and the design of Network Interfaces. Will also discuss the evaluation mechanism of NoC architectures.
3. **Router Design and Performance Evaluation (20 minutes):** Will present the router design strategies followed in NoCs. It will deliberate on clocking strategies, FIFO design, Globally Asynchronous Locally Synchronous (GALS) style of communication, router architecture design for both single- and virtual-channel wormhole routers, adaptive and application-specific router design, etc. Will contain the evaluation mechanism of NoC architectures, simulator design, performance evaluation and comparison between different NoC structures.
4. **Application Mapping (20 minutes):** Will present the application mapping strategies followed in NoCs. Given an application task graph, several mapping strategies have been developed to associate the IPs carrying out these tasks with the routers. This portion of the talk will enumerate various strategies like, ILP, constructive and iterative heuristics, meta-search techniques etc. for the mapping problem.
5. **Application-Specific NoC Design (30 minutes):** Will discuss on the problem of synthesizing application specific NoCs. The NoC synthesis problem addresses the issue of evolving the best possible NoC topology for a given application task graph. It will include the issues like topology generation, scheduling algorithm development on the designed topology, router placement, etc. It will also include the floorplan generation techniques along with core and router placement for NoC synthesis.
6. **Reconfigurable NoC Design (30 minutes):** Will deal with reconfigurable NoC design issues. The subtopics include using FPGA for NoC reconfiguration, designing a router architecture that will aid in dynamic change of interconnection pattern between the routers, reconfigurable link design and will revisit the application mapping problem and the topology synthesis from the reconfiguration viewpoint.
7. **3D NoC (20 minutes):** Will highlight the limited floorplanning choices of 2-D NoC and also focus on 3-D NoC design which is the amalgamation of 2-D NoC and 3-D IC. In 3-D IC, multiple layers of active silicon are stacked using special vertical interconnects, known as *through-silicon-via* (TSV). The actual benefit of 3-D IC relies on the fact that the relatively long wires (~mm) of 2-D IC can be replaced by these TSVs whose lengths are about tens of microns. This portion will explore the design space of integrating multiple cores onto different silicon layers focusing on the performance and cost metrics.
8. **Thermal Aware NoC Design (20 minutes):** Will discuss about the need for the thermal awareness in NoC design. It will include the topics like thermal aware application mapping, NoC synthesis techniques. It will also include the thermal management techniques in 3-D environment as well.
9. **Conclusion and Discussions (10 minutes).**

Technical Bibliography:

Papers published by the authors:

Journal Papers:

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6. P.K. Sahu, S. Chattopadhyay, *A Survey on Application Mapping Strategies for Network-on-Chip Design*, Journal of Systems Architecture (Elsevier), Vol. 59, 2013, pp. 60-76.

7. S. Kundu, J. Soumya, S. Chattopadhyay, *Design and Evaluation of Mesh-of-Tree based Network-on-Chip using Virtual Channel Router*, Microprocessors and Microsystems (Elsevier), Vol. 36, No. 6, 2012, pp. 471-488.
8. S. Kundu and S. Chattopadhyay, *Network-on-Chip Architecture Design Based On Mesh-of-Tree Deterministic Routing Topology*, International Journal of High Performance Systems Architecture, Vol-1, No-3, 2008, pp. 163-182.
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Conference Papers:

1. Soumya J., P. Venkatesh, S. Chattopadhyay, *Flexible Router Placement with Link Length and Port Constraints for Application Specific Network on Chip Synthesis*, IEEE International Symposium on VLSI (ISVLSI) 2011.
2. Soumya J., A. Sharma, S. Chattopadhyay, *A Locally Reconfigurable Network-on-Chip Architecture and Application Mapping onto it,* 18th IEEE VLSI Design and Test Symposium (VDAT), 2014 (Accepted).
3. N Chatterjee, N Prasad, S Chattopadhyay, *A Spare Link Based Reliable Network -on-Chip Design*, 18th International Symposium on VLSI Design and Test (VDAT), 2014 (Accepted).
4. N Prasad, M R Tripathy, A D Das, N R Behera, A K Swain, Efficient VLSI Implementation of CORDIC Based Direct Digital Synthesizer, International Conference on Intelligent Computing, Communication, and Devices (ICCD), 2014.
5. N Prasad, A K Swain, K K Mahapatra, Design and Error Analysis of a Scale Free CORDIC Unit with Corrected Scale Factor, IEEE Asia Pacific Conference on Post Graduate Research in Microelectronics and Electronics (PrimeAsia), 2012.
6. S. Kundu, K. Manna, S. Gupta, R. Parikh, S. Chattopadhyay, *A Comparative Performance Evaluation of Network-on-Chip Architectures under Self-Similar Traffic*, IEEE International Conference on Advances in recent Technologies in Communication and Computing (ARTCom), 2009.
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8. S. Kundu, R. Dasari, K. Manna, S. Chattopadhyay, *A Comparison of Virtual Cut-Through and Wormhole Switching in Mesh-of-Tree Topology based Network-on-Chip*, CSI-RDHS 2008, India.
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13. S. Kundu, M. Sathi, S. Chattopadhyay, *Genetic Algorithm Based Test Scheduling for Network-on-Chip*, 11th IEEE VLSI Design and Test Symposium, Kolkata, India 2007.
14. K. Manna, S. Chattopadhyay, I.Sengupta, *Performance evaluation of a novel Dimension Order Routing algorithm for Mesh-of-tree based Network-on-Chip architecture*, 1st International Conference on Parallel Distributed and Grid Computing (PDGC), pp.135-139, 28-30 Oct. 2010.
15. K. Manna, S. Chattopadhyay, I.Sengupta, *A Novel Deadlock-Free Shortest-Path Dimension Order Routing Algorithm for Mesh-of-Tree Based Network-on-Chip Architecture*, Advances in Computer Science and Information Technology, Communications in Computer and Information Science, Springer Berlin Heidelberg, Vol. 131, pp. 168-178, 2011.
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21. P. K. Sahu, P. Venkatesh, S. Gollapalli, S. Chattopadhyay, *Application Mapping onto Mesh Structured Network-on-Chip using Particle Swarm Optimization*, IEEE International Symposium on VLSI (ISVLSI), 4-6 July. 2011.

Also a very detailed list of related papers till 2009 can be found at **http://www.cl.cam.ac.uk/~rdm34/onChipNetBib/onChipNetwork.pdf**. This, added with the papers recently surveyed by the research group, as included in various publications from the group (noted earlier) will form the full technical bibliography.

Tutorial Materials: Copies of lecture slides.

Biography:

Soumya J. received her *B.Tech* degree in *Electronics and Communications Engineering* from *Jawaharlal Nehru Technological University*, *Hyderabad* in 2007 and *M.Tech* degree in *Visual Information and Embedded Systems* from *Indian Institute of Technology, Kharagpur* in 2010. She is currently working towards *PhD* degree in *Department of E&ECE*, *IIT Kharagpur*. Her research interests include *Application Specific Network on Chip* and *Reconfigurable Network-on-Chip design.* She has published papers in reputed international journals and conferences. She is a graduate student member of *IEEE*, *IEEE Computer Society* and *IEEE Women In Engineering* (*WIE*).

Prasad N. received his *B.Tech.* degree in *Electronics and Communication Engineering* from *Jawaharlal Nehru Technological University*, *Hyderabad* in 2011 and *M.Tech.* degree in *VLSI Design and Embedded Systems* from *National Institute of Technology, Rourkela* in 2013. He is currently working towards *PhD* degree in *Department of E&ECE*, *IIT Kharagpur*. His research interests include *Application Specific Network on Chip Architectures, FPGA Architectures for Signal Processing,* and *Reconfigurable Network-on-Chip Architecture Design.* He has published papers in reputed international conferences.

Santanu Chattopadhyay received his *BE* degree in *Computer Science and Technology* from *Calcutta University (B.E. College)* in 1990. He received his *M.Tech* degree in *Computer and Information Technology* from *Indian Institute of Technology, Kharagpur* in 1992. He also did his *PhD* from the same institute in 1996 in *Computer Science and Engineering*. He is currently a Professor in the *Dept. of Electronics and Electrical Communication Engineering, IIT Kharagpur*. His research interests include *Network-on-Chip Design and Test, Low-power VLSI Design and Test, Fault Diagnosis*, etc. He is in the Editorial Board of the *IET Journals – Circuits, Devices & Systems*. He has published more than 150 papers in reputed refereed international journals and conferences. He has coauthored a book on *Additive Cellular Automata – Theory and Applications (Vol. 1)*, published by the *IEEE Computer Society Press, USA*, and has written text books on *Compiler Design*, *System Software*, *Embedded System Design (Ed.2)*, published by the *PHI Learning, India*. He has received the *Supreme Engineering Award, 2012*, for being judged the *Best Faculty in Engineering*. He has presented the following tutorials on related topics, earlier.

- Tutorial presentation in *Emerging Applications of Information Technology* (*EAIT*)*, 2011* held at Birla Institute of Technology, Meshra (Kolkata Campus). Topic: Network-on-Chip – The Next Generation of Multi-Processor System-on-Chip, Duration: 2 Hours, Presenters: S. Kundu and S. Chattopadhyay.
- Tutorial presentation in *VLSI Design and Test Symposium* (*VDAT*)*, 2010* held at Chitkara University, Chandigarh. Topic: Network-on-Chip – The Next Generation of Multi-Processor System-on-Chip, Duration: 3 Hours, Presenters: S. Kundu and S. Chattopadhyay.
- Tutorial presentation in *Advanced Computing and Communication Conference* (*ADCOM*)*, 2009* held at Indian Institute of Science (IISc), Bangalore. Topic: Network-on-Chip – The Next Generation of Multi-Processor System-on-Chip Duration: 4 Hours, Presenters: S. Kundu and S. Chattopadhyay.